Latin-American alliance for capacity building in advanced physics

LA-CoNGA physics

Módulo de Instrumentación

Introducción a los Sistemas de Medida

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Contents

Introduction to Measuring systems

- Sampling Theory
- The Nyquist criteria
- ADC Converter specifications
- Time to Digital Converters
- Example: Analog conversion with Arduino

Sampling Theory

- A block diagram of a typical realtime sampled data system is shown
- Prior to the actual analog-to-digital conversion, the analog signal usually passes through some sort of signal conditioning circuitry which performs such functions as amplification, attenuation, and filtering

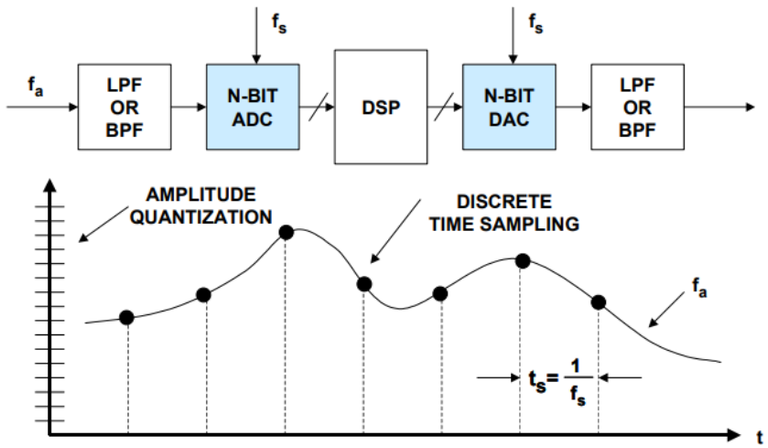

Figure 1: Sampled Data System

- The lowpass/bandpass filter is required to remove unwanted signals outside the bandwidth of interest and prevent aliasing.

Sampling Theory

- The System shown is a **real-time system**, i.e., the signal to the ADC is continuously sampled at a rate equal to f_s,
- the ADC presents a new sample to the DSP at this rate.
- In order to maintain real-time operation, the DSP must perform all its required computation within the sampling interval, $1/f_s$, and present an output sample to the DAC before arrival of the next sample from the ADC.
- An example of a typical DSP function would be a digital filter.
- Note that the DAC is required only if the DSP data must be converted back into an analog signal
- There are two key concepts involved in the actual analog-to-digital and digital-to-analog conversion process:
  - discrete time sampling
  - finite amplitude resolution

The Need for a Sample-and-Hold Amplifier (SHA) Function

- For this discussion we assume that the input signal has some upper frequency limit f_a.
- Most ADCs today have a built-in sample-and-hold function, thereby allowing them to process *AC* signals.

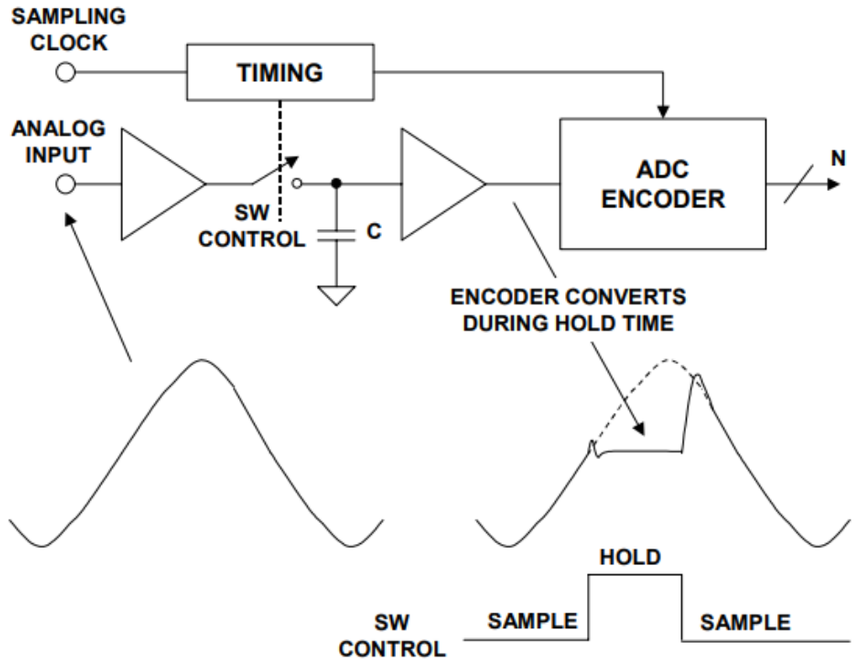

Figure 2: Sample-and-Hold Function Required for Digitizing AC Signals

Sample and hold circuit

- The ideal SHA is simply a switch driving a hold capacitor followed by a high input impedance buffer.
- The input impedance of the buffer must be high enough so that the capacitor is discharged by less than 1 LSB during the hold time.
- The SHA samples the signal in the sample mode, and holds the signal constant during the hold mode.
- The timing is adjusted so that the encoder performs the conversion during the hold time.

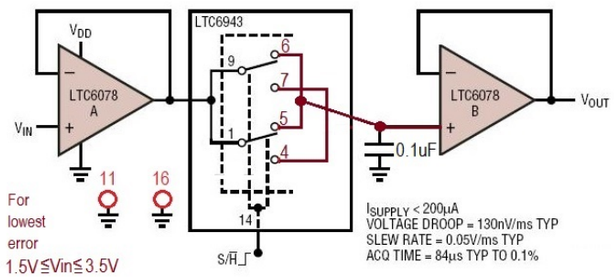

Figure 3: Actual Sample-and-Hold Amplifier

- A sampling ADC can therefore process fast signals—the upper frequency limitation is determined by:
  - SHA aperture jitter
  - bandwidth
  - distortion

The Nyquist Criteria

- A continuous analog signal is sampled at discrete intervals, $t_s = 1/f_s$,which must be carefully chosen to ensure an accurate representation of the original analog signal
- It is clear that the more samples taken **(faster sampling rates)**, the more accurate the digital representation
- But if fewer samples are taken **(lower sampling rates)**, a point is reached where critical information about the signal is actually lost

The Nyquist Criteria

Simply stated, the Nyquist criteria requires that the sampling frequency be at least twice the highest frequency contained in the signal, or information about the signal will be lost.

- If the sampling frequency is less than twice the maximum analog signal frequency, a phenomena known as **aliasing** will occur.
- A signal with a maximum frequency f_a must be sampled at a rate $f_s > 2fa$ or information about the signal will be lost because of aliasing.

Aliasing: time domain

Consider the case of a single frequency sine wave of frequency f_a sampled at a frequency f_s by an ideal impulse sampler

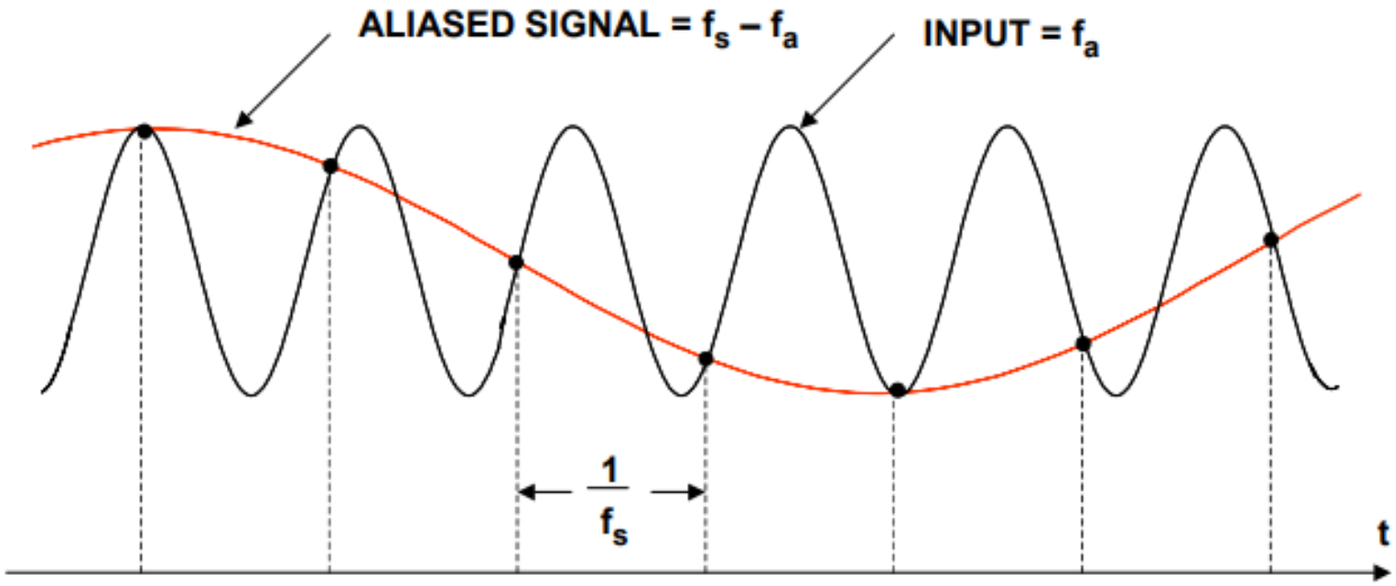

Figure 4: Aliasing in the Time Domain- **NOTE: f_a IS SLIGHTLY LESS THAN f_s**

Aliasing: frequency domain

The frequency-domain output of the sampler shows aliases or images of the original signal around every multiple of f_s

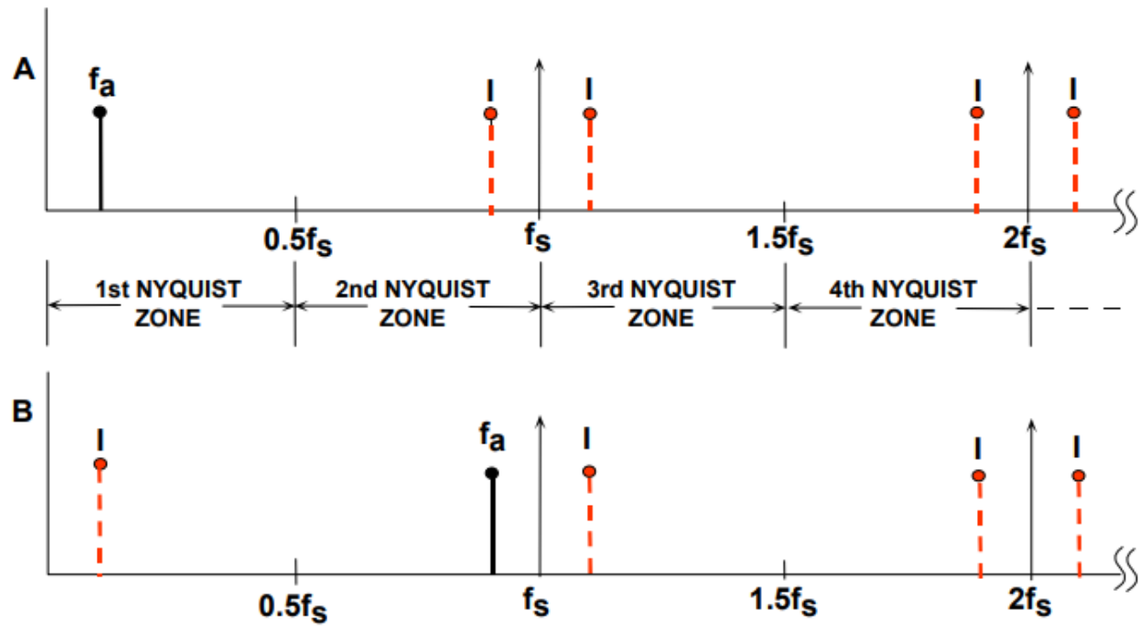

Figure 5: Analog signal sampled with images at $|\pm Kf_s \pm Kf_a|$ $K = 1, 2, 3, ...$

ADC specifications

Absolute Accuracy Error

Absolute accuracy error of an ADC at a given output code is the difference between the actual and the theoretical analog input voltages required to produce that code.

- Since the code can be produced by any analog voltage in a finite band, the "input required to produce that code" is usually defined as the midpoint of the band of inputs that will produce that code.
- For example, if $5V$, $\pm 1.2mV$, will theoretically produce a 12-bit half-scale code of 1000 0000 0000, then a converter for which any voltage from $4.997V$ to $4.999V$ will produce that code will have absolute error of $(1/2)(4.997 + 4.999)\check{}5V = +2mV$
- Sources of error include gain (calibration) error, zero error, linearity errors, and noise. Absolute accuracy measurements should be made under a set of standard conditions with sources and meters traceable to an internationally accepted standard.

ADC specifications

Accuracy Relative

Relative accuracy error, expressed in %, ppm, or fractions of 1 LSB, is the deviation of the analog value at any code (relative to the full analog range of the device transfer characteristic) from its theoretical value (relative to the same range), after the full-scale range (FSR) has been calibrated

- Since the discrete analog values that correspond to the digital values ideally lie on a straight line, the specified worst case relative accuracy error of a linear ADC or DAC can be interpreted as a measure of end-point nonlinearity

Acquisition Time

The acquisition time of a SHA circuit for a step change is the time required by the output to reach its final value, within a specified error band, after the sample command has been given

- Included are switch delay time, the slewing interval, and settling time for a specified output voltage change

ADC specifications

Aliasing

A signal within a bandwidth fa must be sampled at a rate fs $>$ 2fa in order to avoid the loss of information

- If $f_s < 2f_a$, a phenomenon called aliasing, inherent in the spectrum of the sampled signal, will cause a frequency equal to $f_s - f_a$, called an alias, to appear
- Since noise is also aliased, it is essential to provide low pass (or band pass) filtering prior to the sampling stage to prevent out-of-band noise on the input signal from being aliased into the signal range and thereby degrading the SNR

Bandwidth (Full linear)

The full-linear bandwidth of an ADC is the input frequency at which the slew-rate limit of the sample-and-hold amplifier is reached.

- Up to this point,the amplitude of the reconstructed fundamental signal will have been attenuated by less than 0.1 dB.
- Beyond this frequency, distortion of the sampled input signal increases significantly

Time to Digital Converters

- The device which converts time interval to measurable digital or binary format is known as time to digital converter TDC.
- The common implementations of the time to digital conversion include counter which increments or decrements on every clock cycle.
- Usually this converter employs crystal to achieve long term stability in the output.

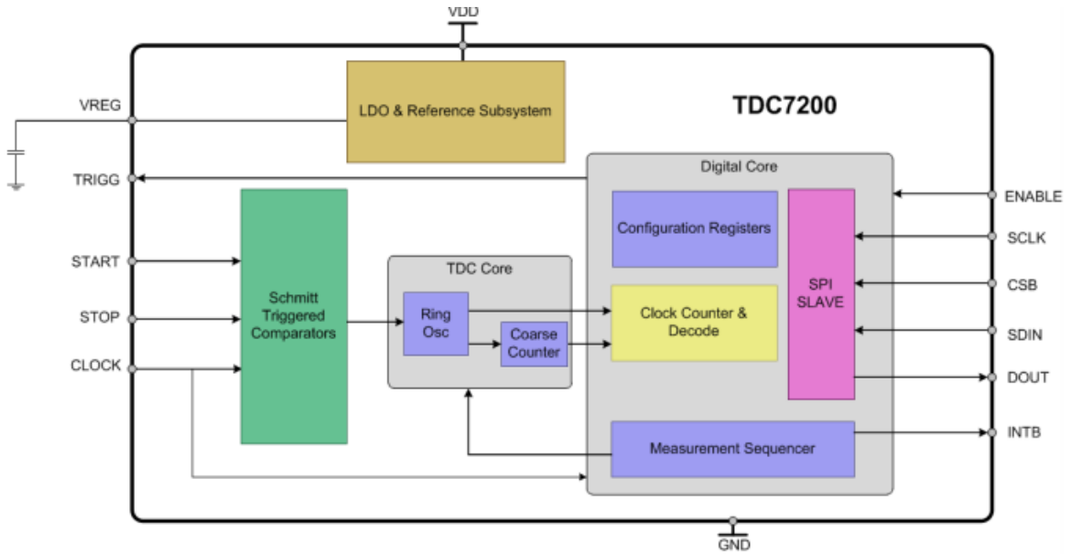

Figure 6: Functional Block Diagram of TDC7200 from TI

Time to Digital Converters

- In most situations, the user wants to measure a time interval, the time between a start event and a stop event.
- That can be done by measuring an arbitrary time both the start and stop events and subtracting. The measurement can be off by two counts.
- The subtraction can be avoided if the counter is held at zero until the start event, counts during the interval, and then stops counting after the stop event.
- Coarse counters base on a reference clock with signals generated at a stable frequency f_0
- When the start signal is detected the counter starts counting clock signals and terminates counting after the stop signal is detected. The time interval T between start and stop is then

$$T = n \cdot T_0 \tag{1}$$

- with n, the number of counts and $T_0 = 1/f_0$ the period of the reference clock.