

# Latin-American alliance for capacity building in advanced physics

## LA-CoNGA physics

### Módulo de Instrumentación

Introducción a los Sistemas de Medida

Dennis Cazar Ramírez

Universidad San Francisco de Quito USFQ

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Latin American alliance for  
Capacity building in Advanced physics  
**LA-CoNGA physics**



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### Introduction to Measuring systems

- ▶ Analog vs Digital signals
- ▶ Digital representation
- ▶ ADC basis
- ▶ ADC errors



## Analog vs Digital Signals

### Analog signal

- ▶ An analog signal is time-varying and generally bound to a range (e.g. +12V to -12V), but there is an **infinite number of values** within that continuous range

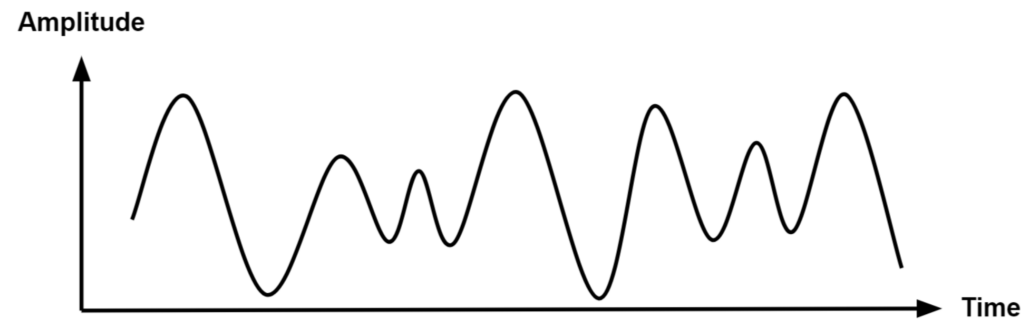


Figure 1: Analog signal Voltage vs time graph

- ▶ When plotted on a voltage vs. time graph, an analog signal should produce a smooth and continuous curve. There should not be any discrete value changes
- ▶ The world is analog



## Analog vs Digital Signals

### Digital signal

- ▶ A digital signal represents data as a sequence of discrete values. A digital signal can only take on one value from a **finite set of possible values** at a given time.

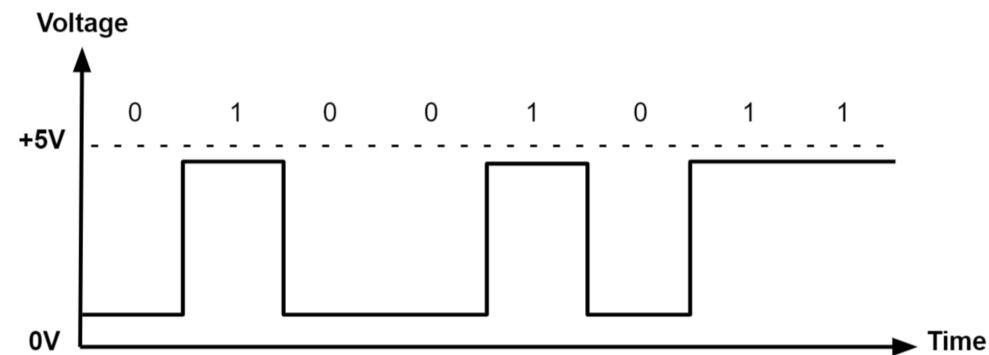


Figure 2: Digital signal Voltage vs time graph

- ▶ When plotted on a voltage vs. time graph, digital signals are one of two values, and are usually between 0V and VCC (usually 1.8V, 3.3V, or 5V)
- ▶ We can represent the world as digital data



## Analog to Digital Conversion

- ▶ Analog-to-digital converters (ADCs) translate analog quantities, which are characteristic of most phenomena in the "real world," to digital language, used in information processing, computing, data transmission, and control systems.

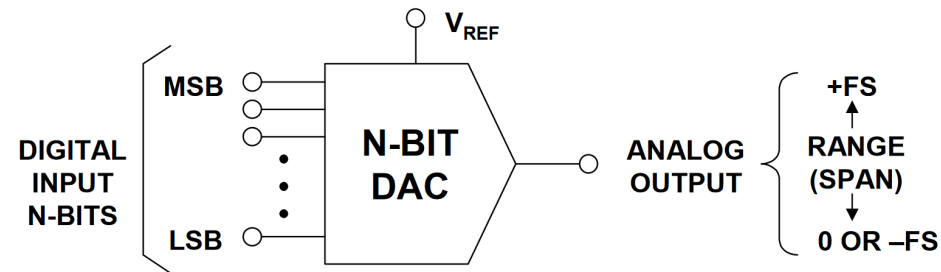


Figure 3: ADC Input and Output definitions

- ▶ As part of the process, the voltages and currents are "normalized" to ranges compatible with assigned ADC input ranges.
- ▶ Analog output voltages or currents from DACs are direct and in normalized form, but they may be subsequently post-processed (e.g., scaled, filtered, amplified, etc.).



## Digital signals

- ▶ Information in digital form is normally represented by arbitrarily fixed voltage levels referred to "ground," either occurring at the outputs of logic gates, or applied to their inputs.
- ▶ The digital numbers used are all basically binary; that is, each "bit," or unit of information has one of two possible states. These states are "off," "false," or "0," and "on," "true," or "1."
- ▶ It is also possible to represent the two logic states by two different levels of current, however this is much less popular than using voltages.
- ▶ There is also no particular reason why the voltages need be referenced to ground—as in the case of emitter-coupled-logic (ECL), positive-emitter-coupled-logic (PECL) or low-voltage-differential-signaling logic (LVDS) for example.

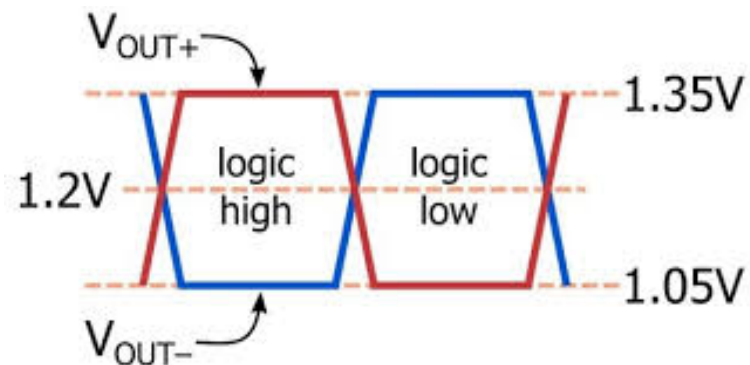


Figure 4: Voltage level and digital equivalent for a LVDS signal



## Digital words

- ▶ A unique parallel or serial grouping of digital levels, or a number, or code, is assigned to each analog level which is quantized (i.e., represents a unique portion of the analog range). A typical digital code would be this array:

$$a_7 a_6 a_5 a_4 a_3 a_2 a_1 a_0 = 10111001 \quad (1)$$

- ▶ It is composed of eight bits. The "1" at the extreme left is called the "most significant bit" (MSB, or Bit 1), and the one at the right is called the "least significant bit" (LSB, or bit N: 8 in this case)
- ▶ The meaning of the code, as either a number, a character, or a representation of an analog variable, is unknown until the code and the conversion relationship have been defined
- ▶ The subscripts correspond to the power of 2 associated with the weight of a particular bit in the sequence.







## Digital codes

BASE 10 NUMBER	SCALE	+10V FS	BINARY	GRAY
+15	+FS - 1LSB = +15/16 FS	9.375	1 1 1 1	1 0 0 0
+14	+7/8 FS	8.750	1 1 1 0	1 0 0 1
+13	+13/16 FS	8.125	1 1 0 1	1 0 1 1
+12	+3/4 FS	7.500	1 1 0 0	1 0 1 0
+11	+11/16 FS	6.875	1 0 1 1	1 1 1 0
+10	+5/8 FS	6.250	1 0 1 0	1 1 1 1
+9	+9/16 FS	5.625	1 0 0 1	1 1 0 1
+8	+1/2 FS	5.000	1 0 0 0	1 1 0 0
+7	+7/16 FS	4.375	0 1 1 1	0 1 0 0
+6	+3/8 FS	3.750	0 1 1 0	0 1 0 1
+5	+5/16 FS	3.125	0 1 0 1	0 1 1 1
+4	+1/4 FS	2.500	0 1 0 0	0 1 1 0
+3	+3/16 FS	1.875	0 0 1 1	0 0 1 0
+2	+1/8 FS	1.250	0 0 1 0	0 0 1 1
+1	1LSB = +1/16 FS	0.625	0 0 0 1	0 0 0 1
0	0	0.000	0 0 0 0	0 0 0 0

Figure 6: Unipolar Binary Codes, 4-bit Converter



Transfer function

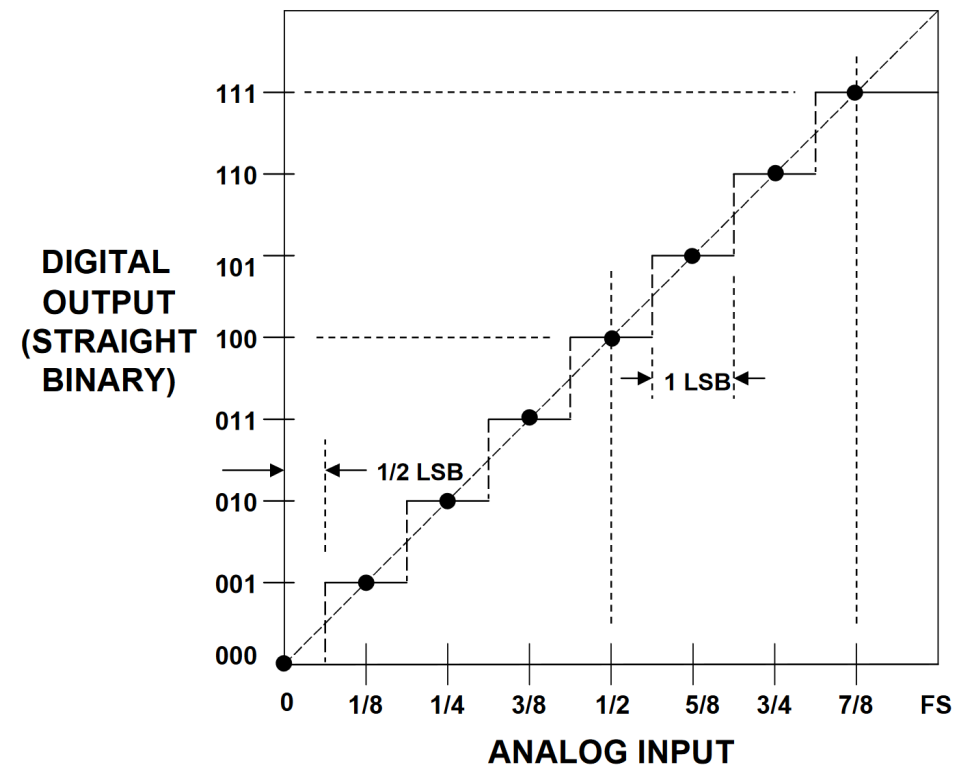


Figure 7: Transfer Function for Ideal Unipolar 3-bit ADC



Transfer function

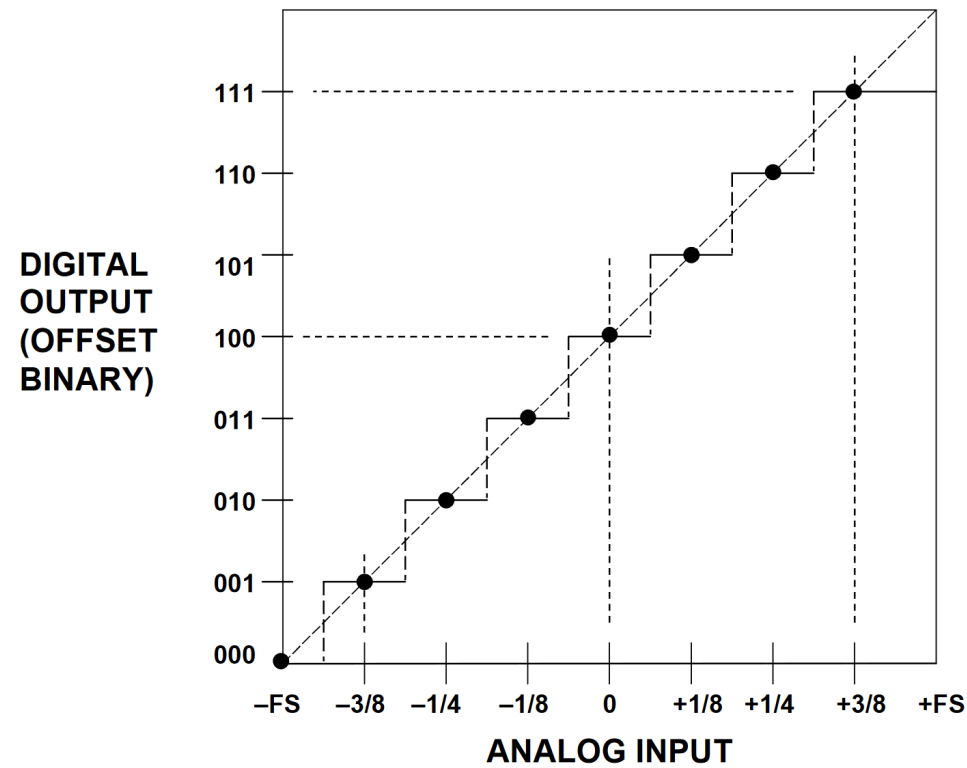


Figure 8: Transfer Function for Ideal Bipolar 3-bit ADC



## Resolution

The resolution of data converters may be expressed in several different ways: the weight of the Least Significant Bit (LSB), parts per million of full-scale (ppm FS), millivolts (mV),

RESOLUTION N	$2^N$	VOLTAGE (10V FS)	ppm FS	% FS	dB FS
2-bit	4	2.5 V	250,000	25	- 12
4-bit	16	625 mV	62,500	6.25	- 24
6-bit	64	156 mV	15,625	1.56	- 36
8-bit	256	39.1 mV	3,906	0.39	- 48
10-bit	1,024	9.77 mV (10 mV)	977	0.098	- 60
12-bit	4,096	2.44 mV	244	0.024	- 72
14-bit	16,384	610 $\mu$ V	61	0.0061	- 84
16-bit	65,536	153 $\mu$ V	15	0.0015	- 96
18-bit	262,144	38 $\mu$ V	4	0.0004	- 108
20-bit	1,048,576	9.54 $\mu$ V (10 $\mu$ V)	1	0.0001	- 120
22-bit	4,194,304	2.38 $\mu$ V	0.24	0.000024	- 132
24-bit	16,777,216	596 nV*	0.06	0.000006	- 144

Figure 9: 10-bits and 10V FS yields an LSB of 10mV, 1000ppm, or 0.1%.

600nV is the Johnson Noise in a 10kHz BW of a 2.2k $\Omega$  Resistor at 25°C



## ADC errors

- ▶ The four **dc errors** in a data converter are
  - ▶ Offset error
  - ▶ Gain error,
  - ▶ Differential linearity error
  - ▶ Integral linearity error

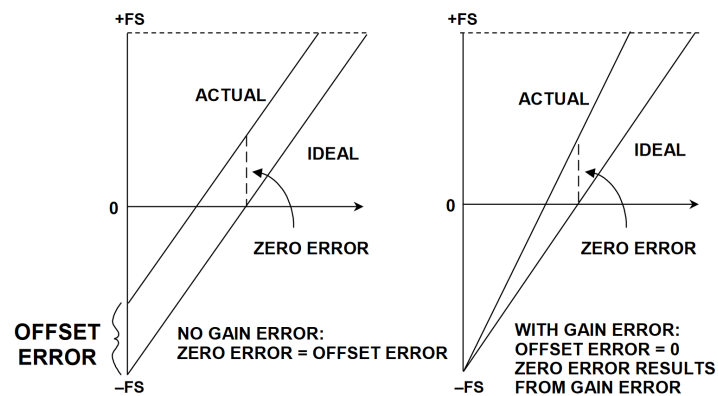


Figure 10: Bipolar Data Converter Offset and Gain Error

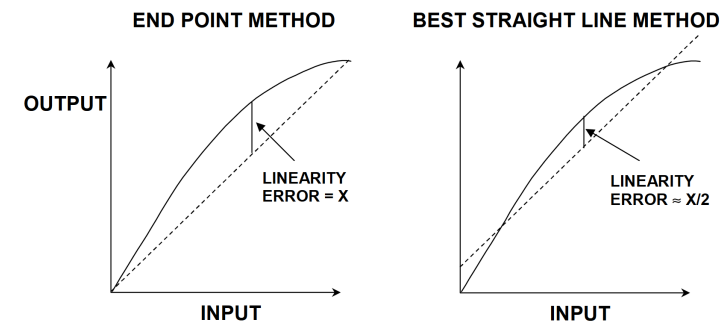
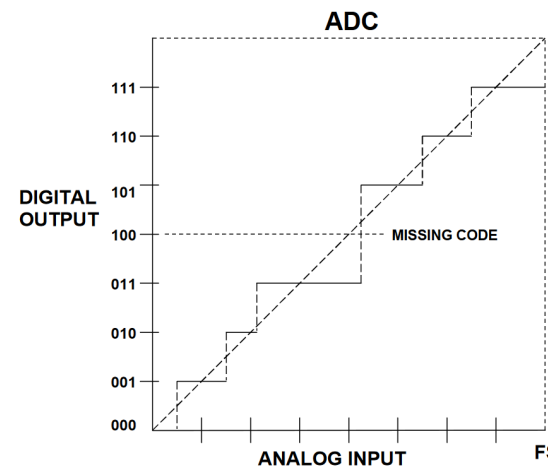


Figure 11: Method of Measuring Integral Linearity Errors (Same Converter on Both Graphs)



## Differential Non linearity

- ▶ The other type of converter nonlinearity is differential nonlinearity (DNL). This relates to the linearity of the code transitions of the converter.



- ▶ In the ideal case, a change of 1 LSB in an ADC there should be exactly 1 LSB change of analog input to move from one digital transition to the next.
- ▶ **Differential linearity error** is defined as the maximum amount of deviation of any quantum (or LSB change) in the entire transfer function from its ideal size of 1 LSB.



DNL details

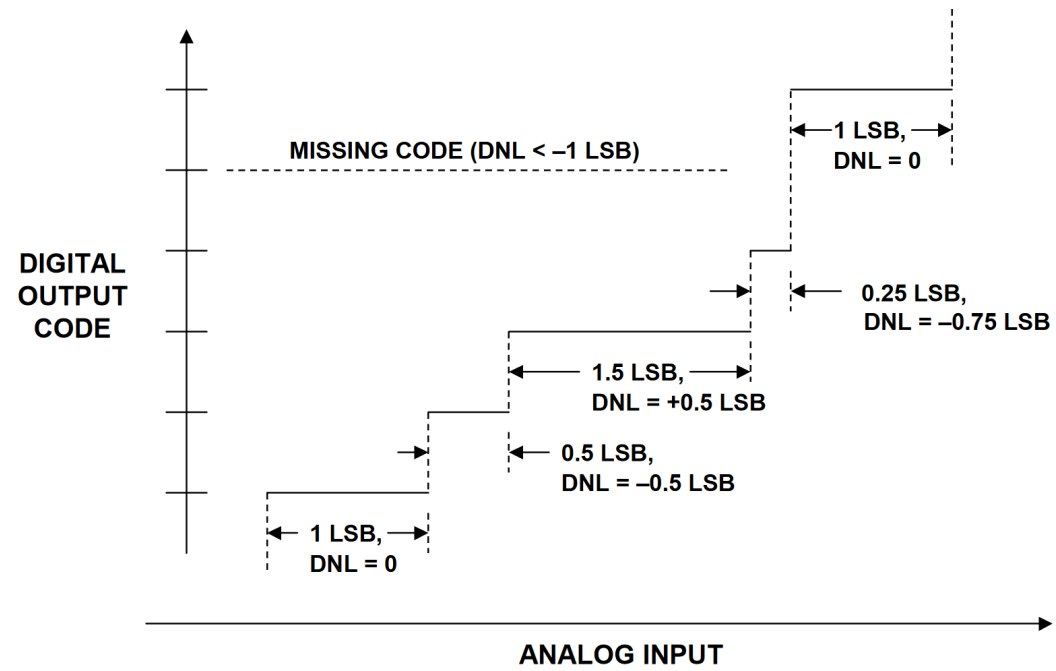


Figure 12: Details of ADC Differential Nonlinearity







Combined effects

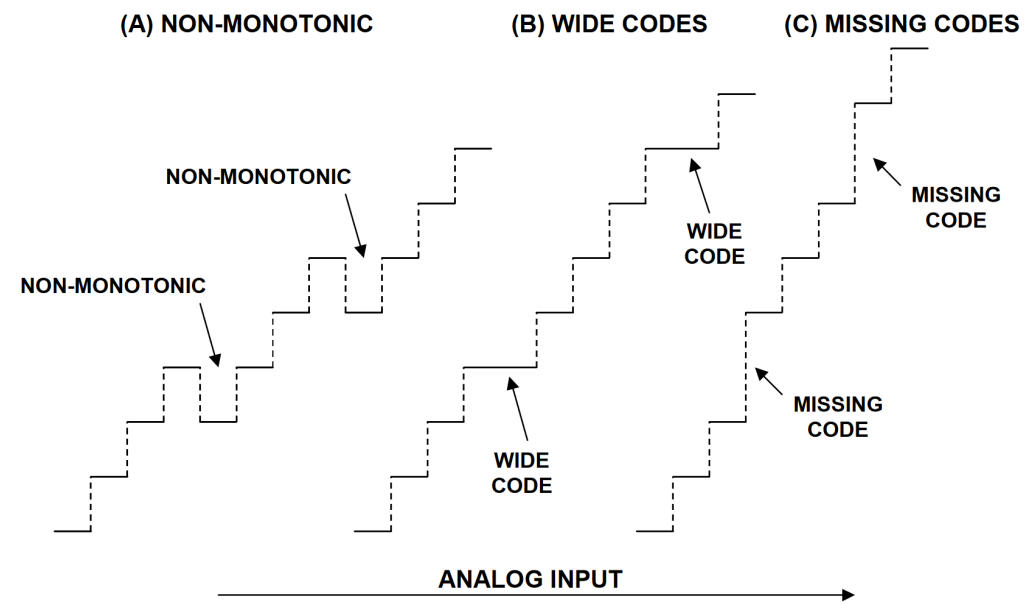


Figure 14: Errors Associated with Improperly Trimmed Subranging ADC



Combined effects

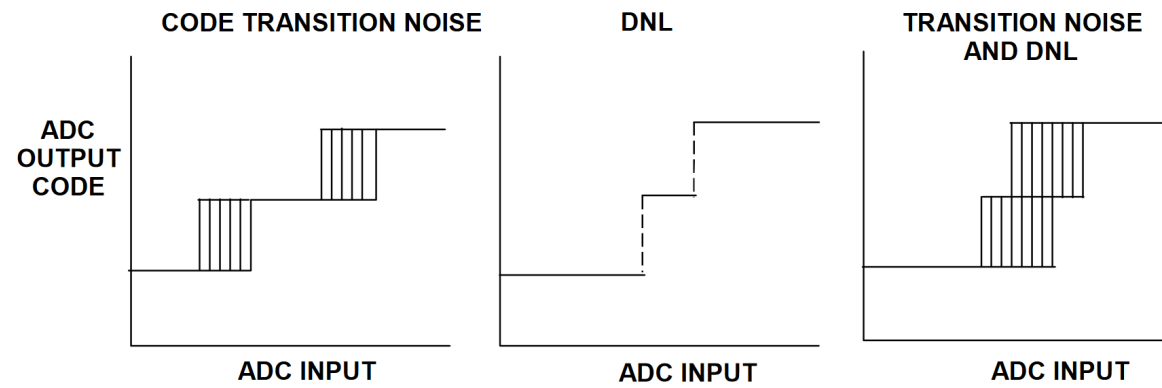


Figure 15: Combined Effects of Code Transition Noise and DNL